REMARKS

The Examiner objected to the abstract, stating "The abstract of the disclosure is objected to because the abstract contains the language of claim 1 and lacks narrative format. Correction is required. See MPEP § 608.01(b)." In response Applicants have replaced the abstract with an abstract in narrative format. However, Applicant have carefully read MPEP § 608.01(b) and find no rule prohibiting the abstract from mimicking claim 1 or any other claim.

The Examiner objected to claims 17-30 because of the following alleged informalities: the preamble should be written as "the computer system" instead of "the system" for correct antecedent basis. In response, Applicants have amended claims 17-30 to include "the computer system."

The Examiner rejected claims 12 and 27 under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the enablement requirement.

The Examiner rejected claims 5 and 20 under 35 U.S.C. §112, second paragraph, as allegedly failing to set forth the subject matter which applicant(s) regard as their invention.

The Examiner rejected claims 1-30 under 35 U.S.C. §102(b) as allegedly being anticipated by Osann et al., JR. *et al.* (Osann et al.) (US 2002/0010903).

Applicants respectfully traverse the §112 and §102 rejections with the following arguments.

35 U.S.C. §112

As to claims 12 and 27, the Examiner states As failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The subject "programmable logic device is connectable between an input , output or both of state machine" is not described in specification.

Applicants contend, the examiners rejection of claims 12 and 27 are moot in light of Applicants amendment of claims 12 and 27 which are supported in one example, by Applicants FIG. 2D and corresponding description on page 6, lines 7 through 16.

As to claims 5 and 20, the Examiner states "Refer to PG Pubs (US 2005/0120323) page 3, ¶ 28, line 3-4, applicant has stated "the FPGA netlist compiled into a SRAM configuration pattern", and this statement indicates that the invention is different from what is defined in the claim(s) because programmable logic device can not be compiled into a pattern. Applicant should revise the claims language for consistent to specification.

Applicants contend, the examiners rejection of claims 12 and 27 are moot in light of Applicants amendment of claims 12 and 27 which adds the word "netlist" as the Examiner has suggested.

35 U.S.C. §102

As to claims 1 and 16, the Examiner states "Osann et al. discloses ....a) modifying a high-level design of said state machine (logic block) to obtain a modified high- level design of said state machine with a modified function (pg. 3, ¶ 39, ll. 5-14); b) generating a programmable logic device netlist from differences in said high-level design and said modified design (pg. 3, ¶ 48, ll. 1-9; ¶ 52, ll. 3-9); and (c) installing (loading) said modified function into said state machine by programming said programmable logic device based on said programmable logic device netlist (pg. 4, ¶152, ll. 3-13).

Applicants respectfully contend that Osann et al. does not anticipate claims 1 and 16, because Osann et al. does not teach each and every feature of claims 1 and 16

In a first example, Osann et al. does not teach "modifying a high-level design of said state machine to obtain a modified high-level design of said state machine with a modified function."

While the statement "First, the designer (user) defines the planned functionality for the ASIC as a whole, including the functionality that the designer believes will be required for the particular reconfigurable logic block, such as a state machine. The designer designates that portion of the functionality that is to be reconfigurable, and software next takes the specified description of the designated functionality to model a PLA structure suitable for implementation of that reconfigurable logic" of Osann et al. paragraph [0039] lines 5-14 appears to teach "modifying a high-level design of said state machine to obtain a modified high-level design of said state machine with a modified function" one must look further for enablement of this statement, which is presented in the context of a summary to truly understand what Osann et al. is actually teaching. This enablement is found is in FIG. 9 and the corresponding description of

FIG. 9 on page 3, paragraph 42 of Osann et al.. et al.

Applicants respectfully point out that, in FIG. 9 and the corresponding description of FIG. 9 on page 3, paragraph 42, Osann et al. is teaching converting (step 1104) a high-level design of a state machine (1102) into programmable logic device format file (1106) not into "a modified high-level design of said state machine" as Applicants claims 1 and 16 require. Further, there is no mention of Osann et al. et als. programmable logic device format file (1106) having " a modified function" from Osann et al. et als. high-level design of a state machine (1102) as Applicants claims 1 and 16 require. In fact, the state machine in PLA format file 1106 of Osann et al. has the same function as the state machine in HDL format 1102.

In a second example, Osann et al. does not teach "generating a programmable logic device netlist from differences in said high-level design and said modified high-level design."

Applicants respectfully point out that, in FIG. 9 and the corresponding description of FIG. 9 on page 3, paragraph 48. Osann et al. is teaching generating (step 1110) a PLA netlist (1112) from a PLA format file (1106) and not from a high-level design and certainly not from "said modified high-level design" as Applicants claims 1 and 16 require Further, since the functions of both HDL design 1102 and PLA design 1106 are the same, it is impossible for Osann et al. to generate a netlist from "differences in said high-level design and said modified high-level design as Applicants claims 1 and 16 require.

Additionally, Applicants respectfully point out that, in FIG. 10 and the corresponding description of FIG. 10 on page 4, paragraph 52. Osann et al. is teaching converting (step 1104) a new high-level design of a state machine (1102') into programmable logic device format file (1106') and not "generating a programmable logic device netlist from differences in said high-

level design and said modified high-level design" as Applicants claims 1 and 16 require. Applicants fail to find any connection between high-level design of a state machine (1102) and new high-level design of a state machine (1102') in Osann et al., other than in on page 4, paragraph 52 where Osann et al. states "the new DDL description of the new PLA functionality 1102' will be converted 1104 to create a PLA format file 1106', similar to that done in FIG. 9".

Stated more succinctly, Osann et al. teaches always a processing an entire HDL file (file 1102 and file 1102') while Applicants claim processing only the difference between two HDL files (the "high-level design" and the "modified high-level design)."

Based on the preceding arguments, Applicants respectfully maintain that Osann et al. does not anticipate claims 1 and 16, and that claims 1 and 16 are in condition for allowance. Since claims 2-15 depend from claim 1 and claims 17-30 depend from claim 16, Applicants contend that claims 2-15 and 17-30 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0457.

Respectfully submitted,
FOR: Goodnow et al.

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